REMARKS

In the Office Action of September 30, 2005, claims 15-17 and 20-24 were rejected under 35 U.S.C. 103(a) as unpatentable over Ito et al. (U.S. Patent No. 6,683,767) in view of Koshikawa et al. (U.S. Patent No. 5,319,302). Claims 1-14, 25 and 26 have been withdrawn and claims 18 and 19 have been cancelled.

Applicants' invention is directed to a voltage regulator that adjusts the operating voltage of an integrated circuit to compensate for the effects of variations in the circuit fabrication process. The voltage regulator includes a voltage down-converter 18 that converts an off-chip supply voltage to an operating voltage that is supplied to the integrated circuit, a signal generator 20 for generating a signal indicative of the desired value of the operating voltage, a detector 22 for measuring at least one electrical or operational parameter of the integrated circuit when the integrated circuit is operated at a nominal voltage, and an evaluator 24 for determining the desired value of the operating voltage based on the parameter(s) measured by the detector and supplying a signal to the signal generator indicative of the desired value.

As the Examiner is aware, the '767 patent discloses a voltage down-converter (150-157) on an integrated circuit. The emphasis in the '767 patent is on the advantageous layout of the integrated circuit so as to accommodate the voltage down converters. Further, the '767 patent discloses a reference voltage generator (60,100) for specifying the desired step-down voltage. At Col. 3, lines 40-42, the '767 patent indicates that the characteristics of generator 100 are determined by trimming information held in an electrically erasable non-volatile memory 135. The Examiner concedes that the '767 patent does not disclose a detector for measuring at least one

electrical or operational parameters of the integrated circuit or an evaluator to determine the desired value of the operating voltage based on parameters measured by the detector. Indeed, the '767 patent teaches away from applicants' invention because it teaches a system in which the output voltage from the voltage down converter is specified by trimming information stored in non-volatile memory rather than by direct read out from the operating integrated circuit.

To make up for the deficiency of the '767 patent, the Examiner points to the use of an internal voltage regulator unit 12 in the semiconductor integrated circuit device of Figs. 5 and 6 of the '302 patent. Further, the Examiner asserts that the internal voltage regulator unit comprises a detector and an evaluator that determines the desired value of the operating voltage based on parameters measured by the detector.

Applicants respectfully disagree. While the '302 patent discloses an integrated circuit having a voltage regulator circuit, the circuit does not include a detector that measures an electrical or operating parameter of the circuit and an evaluator that determines the desired value of the operating voltage based on such measurements and supplies a signal representative of the desired value. Rather, the circuit shown in Figs. 5 and 6 of the '302 patent is a modification of the prior art circuit of Figs. 1-4 so as to add the latch circuit 12i shown in the bottom right-hand corner of Fig. 6. As a result, as explained at Col. 7, lines 26-40 of the '302 patent, a circuit instability is avoided around an abrupt transition region such as at a power voltage level Vcc of 7 volts.

The reference voltage regulator of the '302 patent is shown in detail in Fig. 6. The regulator comprises a preliminary reference voltage generator 12c, a preliminary voltage regulator 12d, a voltage divider 12e that operates as a secondary reference

voltage generator, a controller 12f, first and second main voltage regulators 12g and 12h, and a latching circuit 12i. All of these elements except the latching circuit are described at Col. 9, lines 14-24 as being similar to corresponding elements in Fig. 1 that are described at Col. 1, line 33 through Col. 4, line 12.

The voltage regulator of the '302 patent provides for voltage regulation by two voltage regulators 12g and 12h without abrupt transitions between the outputs of the two regulators. The description of the regulator indicates that the regulator is a series of comparators. In particular, the preliminary voltage regulator (element 2 of Fig. 1 and 12d of Fig. 6) compares the output of the preliminary reference voltage generator with the voltage at reference node N1. (Col. 1, lines 47-52). If the voltage level at node N1 equals the preliminary voltage reference level Vref, the output voltage Vref1 remains constant. If the voltage level at node N1 is less than Vref, the comparator lowers the output voltage and raises the voltage at node N1. If the voltage level at node N1 exceeds Vref, the comparator increases the output voltage and lowers the voltage at node N1. (Col. 1, lines 52-68). As a result, as stated at Col. 2, lines 1-7, the output voltage Vref1 is maintained at a level higher than the preliminary reference voltage level Vref by a predetermined value.

The output voltage Vref1 is supplied to controller 3 of Fig. 1 (element 12 of Fig. 6) which is essentially a switch. Voltage divider 4 (element 12e of Fig. 6) divides the power supply voltage Vcc to produce reference voltages BIV at node N5 and BREF at node N6. As described at Col. 2, lines 56-65 of the '302 patent, if Vref1 is higher than the voltage level BREF, output node 4 goes to a high voltage level and activation signal

BIDM from controller 3 remains low. If, however, BREF is higher than Vref1, output node 4 goes down and signal BIDM goes to the high voltage level.

Main voltage regulator 5 (element 12g of Fig. 6) is a comparator similar to that of regulator 2. The comparator compares the voltage level at node 8 with Vref1 from the output of regulator 2. As stated at Col. 3, lines 4-21, if the voltage level at node 8 is higher than Vref1, the comparator lowers the voltage level at node 8; and if the voltage level at node 8 is lower than Vref1, the comparator raises the voltage level. Thus, the voltage level at node 8 is regulated at the level of Vref1.

Main voltage regulator 6 (element 12h of Fig. 6) is another comparator similar to that of controller 3. When this regulator is activated by signal BIDM, the comparator compares the signal at node N9 with the signal BIV from node N5 of the voltage divider. The comparator operates so that the signal at the output node N9 is regulated at the level of the signal BIV with which it is compared.

As detailed at Col. 3, line 63 to Col. 4, line 12, the outputs from nodes N8 and N9 are coupled to node N10 which, in turn, is coupled to internal power supply unit 7 which regulates an internal power voltage level IVcc. This makes it possible to provide IVcc at a level BREF for testing purposes and at a lower level Vref1 for standard operation.

While the '302 patent discloses a voltage regulator in an integrated circuit, there is no indication that the voltage regulator incorporates a detector for measuring an electrical or operating parameter of the integrated circuit or an evaluator that determines a desired value of the operating voltage based on a parameter measured by the detector and then supplies a signal to a signal generator that is indicative of this value. Thus, the '302 patent does not disclose the features admittedly missing from the '767 patent.

Because the '767 patent is a programmed device while the '302 patent is not, there is also no reason to combine the two references. Indeed, it is not seen how the two references could be combined because the '767 patent teaches a system in which the output of the voltage down converter is a static voltage level specified by the value stored in the electrically erasable non-volatile memory while the '302 patent teaches a system in which the output of the voltage regulator is a dynamically changing signal.

For these reasons, claim 15 is believed to be patentable over the references cited.

Dependent claims 16, 17, 20 and 21 are believed patentable for the same reason claim 15 is patentable.

Independent claim 22 recites a detector that measures at least one electrical or operational parameter of a circuit of the integrated circuit and produces a measurement signal that is used to control the signal generated by the signal generator. Claim 22 is believed patentable over the references because they do not disclose such a detector.

Dependent claims 23 and 24 are patentable for the same reason claim 22 is patentable.

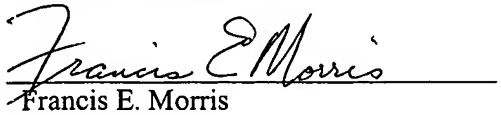
In view of the forgoing remarks, the claims in this application are believed to be in condition for allowance. Such action is respectfully requested. If the Examiner believes a telephone interview would expedite prosecution of this application, she is invited to call applicants' attorney at the number given below.

Aside from the fee for the RCE and an extension of time, no additional fees are believed to be due. However, if a fee is due, the Patent Office is authorized to charge Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 for all required fees for

this reply and any further reply requiring a petition for extension of time for its timely submission. A copy of this sheet is enclosed for such purpose.

Respectfully submitted,

Date: March 30, 2006



Francis E. Morris
Reg. No. 24,615
MORGAN LEWIS & BOCKIUS LLP
Customer No. 048591
(212) 309-6632